Remarks

Claims 1-5, 7-18, and 20-25 are pending in the application. Claims 1-5, 7-12, 14-18 and 20-24 are rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (U.S. Patent No. 6,934,830) ("Kadambi"), in view of Choquette (U.S. Patent No. 6,088,784), in view of Hennessy and Patterson ("Computer Architecture: A Quantitative Approach") ("Hennessy"). Claim 13 is rejected under 35 U.S.C. §103(a) as being unpatentable over Kadambi et al. (US 6,934,830) ("Kadambi") in view of Choquette (U.S. 6,088,784), in view of Hennessy and Patterson ("Computer Architecture: A Quantitative Approach") ("Hennessy"), further in vew of Zaitzeva et al. (U.S. Patent No. 5,781,924) ("Zaitzeva"). Applicants respectfully request reconsideration in view of the following remarks.

Applicants respectfully submit that the cited references do not teach or suggest "[a] processor comprising: ... a register file cache coupled to the register file and to the execution unit, said register file cache including a fill cache and a write-back cache; and a write-back mechanism to move data from the write-back cache of the register file cache to the register file, wherein said fill cache is to store a source operand from the register file if the source operand is not found in the fill cache and the write-back cache (*e.g.*, as described in claim 1).

First, Applicants agree with the Office Action's assertion that Kadambi and Choquette fail to teach a register file cache including a fill cache to the register file; and wherein said fill cache is to store a source operand from the register file if the source operand is not found in the fill cache and the write back cache. *See* Office action dated 4/18/2007, page 4.

The Office Action, however, asserts Hennessey discloses a register file cache including a fill cache and a write back cache, citing pages 403-406 and Figure 5.7. It further asserts "the first data block is the fill cache and the second data block is the write-back cache", without any

further support from the reference. *See* id. Applicants disagree, and submit the current citations are inadequate to support a proper rejection of claim 1.

The Office Action cites to an extensive section of the Hennessey textbook (pages 403-406) and Figure 1, but offers no particularized citations to support its rejection. Applicants submit there is no way to determine which portion of the cited section the Office Action is referring to support its rejection. For example, there is no reference to a "first data block" or a "second data block" anywhere in the cited portion of the Hennessey reference. Similarly, there is no reference to the same anywhere in the Figure 1 of the Hennessey reference or its associated description. *See* page 403. The Hennessey reference includes references to "data blocks" (generally), "victim blocks", and "old data blocks", and generic references to data caches, buffers, and physical addresses, but there is no way to determine whether these references are what the Office Action is referring to. Applicants submit without further citations to clarify the basis for the Office Action's assertion, the current rejection does not support a proper §103 rejection of claim 1.

The Office Action further asserts the cited section of Hennessey teaches data moved from a write-back cache to a register file, citing the same section and the same Figure as those discussed above – pages 403-406 and Figure 1 – without any further citations to the reference. It also asserts "the second data block moves from the cache to the lower-memory." *See* id. This citation fails to support a proper §103 rejection for at least the reasons described above. In particular, there is no mention which second data block, which cache, and which lower-memory the Office Action is referring to, or where exactly the Hennessey reference teaches a second data block moving from a cache to a lower-memory. Applicants submit without further citations or

support to clarify the basis for the Office Action's assertion, the current rejection does not support a proper §103 rejection of claim 1.

Furthermore, the Office Action asserts the cited section of Hennessey teaches a fill cache to store a source operand is not found in the fill cache and the write-back cache, citing again to pages 403-406 and Figure 1 without any further citations to the reference. It further asserts "both data blocks are searched for a hit. If a miss occurs, the data is fetched from lower memory…". *See* id. Again, there are no citations to support there assertions or any explanation of the basis of these assertions as originating from the cited reference. Applicants submit without further citations or support to clarify the basis for the Office Action's assertion, the current rejection does not support a proper §103 rejection of claim 1.

Zaitzeva fails to make up for the deficiencies of Hennessey. Zaitzeva is directed to computer caches methods, and specifically cache misses. However, it does not teach or suggest at least a processor comprising: a register file cache including a fill cache and a write-back cache; and a write-back mechanism to move data from the write-back cache of the register file cache to the register file, wherein said fill cache is to store a source operand from the register file if the source operand is not found in the fill cache and the write-back cache (*e.g.*, as described in claim 1).

In order to support a proper §103(a) rejection, the cited references must teach or suggest all of the claimed limitations. See MPEP §706.02(j). However, for at least the reasons described above, the current rejection fails to cite all of the claimed limitations of independent claim 1 in the references. Therefore, the current §103(a) rejection of claim 1 is lacking and should be withdrawn. Applicants submit claim 1 is presently allowable, and independent claims 4, 15, and

23 are allowable for similar reasons. Claims 2, 5, 7-14, 18, 20-22, and 24 are allowable for depending from an allowable base claim.

Applicants respectfully submit that the present application is in all aspects in allowable condition, and earnestly solicits favorable reconsideration and early issuance of a Notice of Allowance.

The Examiner is invited to contact the undersigned at (408) 975-7950 to discuss any matter concerning this application. The Office is authorized to charge any fees related to this communication to Deposit Account No. 11-0600.

Respectfully submitted,

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